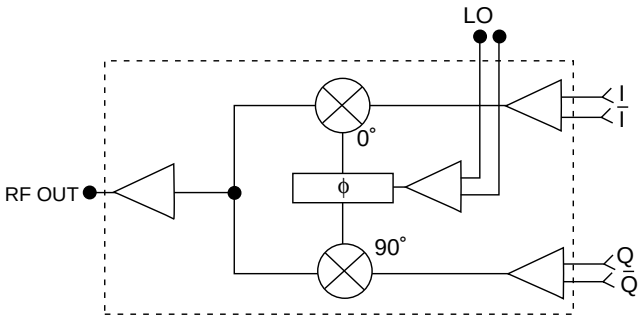
NEC

1 GHz QUADRATURE MODULATOR | UPC8110GR

FEATURES

- **DIRECT MODULATION RANGE:** 800 MHz TO 1 GHz
- **SUPPLY VOLTAGE RANGE:** V_{CC} = 2.7 V to 3.6 V
- **LOW OPERATION CURRENT:** 24 mA Typ
- **LOW CURRENT SLEEP MODE**

FUNCTIONAL BLOCK DIAGRAM



DESCRIPTION

The UPC8110GR is a silicon monolithic integrated circuit designed as a 1 GHz direct quadrature modulator for digital mobile communication systems. The device is manufactured using the NESAT III MMIC process and is housed in a 20 pin plastic SSOP package that contributes to miniaturizing the system. The device has power save function and operates on a 3 V supply voltage for low power consumption.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = 3 V, $V_{PS} \geq$ 2.2 V unless otherwise specified)

PART NUMBER PACKAGE OUTLINE			UPC8110GR S20		
SYMBOLS	**PARAMETERS AND CONDITIONS**	**UNITS**	**MIN**	**TYP**	**MAX**
I_{CC}	Circuit Current (no signal) $V_{PS} \geq$ 2.2 V Circuit Current (power save) $V_{PS} \leq$ 0.5 V	mA μA	15	24	33 10
$P_{O(SAT)}$	Maximum Output Power[1]	dBm		-10	
L_{OL}	LO Carrier Leak[1]	dBc		-35	-30
I_{MR}	Image Rejection[1]	dBc		-40	-30
$IM_{3\ I/Q}$	I/Q 3rd Order Intermodulation Distortion[1]	dBc		-45	-30
$Z_{I/QIN}$	I/Q Input Impedance, single-ended	kΩ		150	
$T_{PS\ (RISE)}$	Power Save Rise Time, $V_{PS} \leq$ 0.5 V to $V_{PS} \geq$ 2.2 V	μs		2	5
$T_{PS\ (FALL)}$	Power Save Fall Time, $V_{PS} \geq$ 2.2 V to $V_{PS} \leq$ 0.5 V	μs		2	5

Note:
1. f_{LOIN} = 948 MHz, P_{LOIN} = -10 dBm, $f_{I/Q}$ = 2.625 kHz, $V_{I/Q} = V_{CC}/2$ (DC)+ 0.5 V_{p-p} (AC).

ABSOLUTE MAXIMUM RATINGS[1] (T_A = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
V_{CC}	Supply Voltage	V	4.0
V_{PS}	Power Save Voltage	V	4.0
P_D	Power Dissipation[2]	mW	430
T_{OP}	Operating Temperature	°C	-40 to +85
T_{STG}	Storage Temperature	°C	-55 to +150

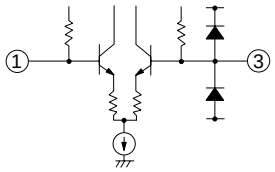
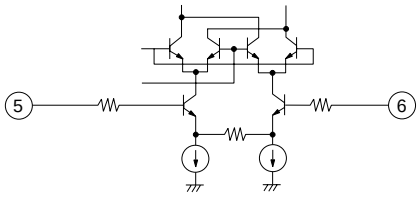
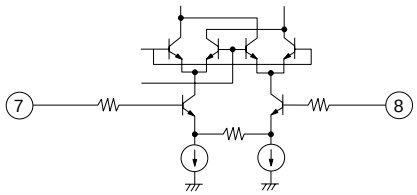
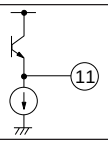
Notes:
1. Operation in excess of any one of these parameters may result in permanent damage.
2. Mounted on a 50 x 50 x 1.6 mm double copper clad epoxy glass PWB (T_A = +85°C).

RECOMMENDED OPERATING CONDITIONS

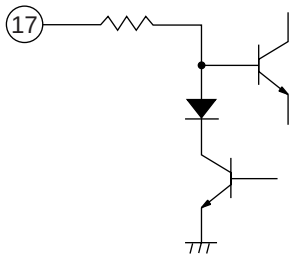
SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
V_{CC}	Supply Voltage	V	2.7	3.0	3.6
V_{PS}	Power Save Voltage	V	0		V_{CC}
T_{OP}	Operating Temperature	°C	-40	+25	+85
P_{LO}	LO Input Power Level	dBm		-10	
f_{LOIN}	LO Input Frequency	MHz	800	900	1000
$f_{I/QIN}$	I/Q Input Frequency	MHz	DC		10
$V_{I/QIN}$	I/Q Input Voltage	mVp-p			500[1]
		mVp-p			250[2]

Notes:
1. Single-ended Input.
2. Differential Input.

PIN FUNCTIONS

Pin No.	Symbol	Supply Voltage (V)	Pin Voltage (V)	Description	Equivalent Circuit
1	LO_{IN}	—	2.6	LO input for the phase shifter.	
2	GND	0	—	Connect to ground with minimum inductance. Track length should be kept as short as possible.	
3	$\overline{LO_{IN}}$	—	2.6	Bypass of the LO input. This pin is grounded through a capacitor of approx. 30 pF.	
4	GND	0	—	Connect to ground with minimum inductance. Track length should be kept as short as possible.	
5	Q	$V_{CC}/2$*1	—	Input for Q signal. If the I/Q input signals are single-ended, the maximum amplitude of the signal is 500 mVp-p.	
6	$\overline{Q}$	$V_{CC}/2$*1	—	Input for Q signal. If the I/$\overline{Q}$ input signals are single-ended, $\overline{Q}$ should be DC biased at V_{CC}/2. If the I/Q input signals are differential, the maximum amplitude of the signal is 250 mVp-p.	
7	$\overline{I}$	$V_{CC}/2$*1	—	Input for I signal. If the I/$\overline{Q}$ input signals are single-ended, $\overline{I}$ should be DC biased at V_{CC}/2. If the I/Q input signals are differential, the maximum amplitude of the signal is 250 mVp-p.	
8	I	$V_{CC}/2$*1	—	Input for I signal. If the I/Q input signals are single-ended, the maximum amplitude of the signal is 500 mVp-p.	
9	GND	0	—	Connect to ground with minimum inductance. Track length should be kept as short as possible.	
10					
11	RF_{OUT}	—	1.6	Output from the modulator. This is an emitter follower output. Connect approx. 15Ω in series to match to 50Ω.	

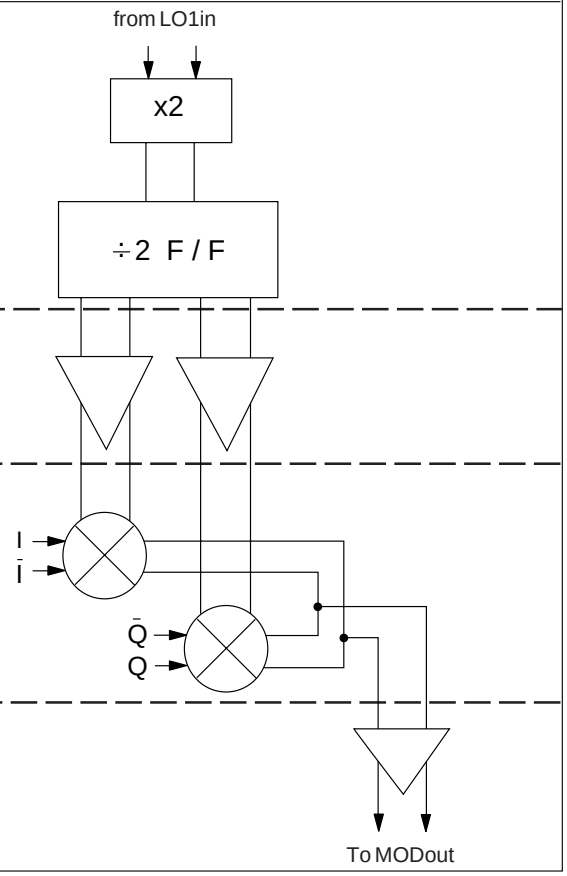
PIN FUNCTIONS

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Supply Voltage</th><th>Pin Voltage</th><th>Description</th><th>Equivalent Circuit</th></tr>
<tr><td>12
13</td><td>GND</td><td>0</td><td>—</td><td>Connect to ground with minimum inductance. Track length should be kept as short as possible.</td><td></td></tr>
<tr><td>14</td><td>V_{CC}</td><td>2.7~
3.6</td><td>—</td><td>Supply voltage pin for the modulator. An internal regulator helps keep the device stable against temperature or V_{CC} variations.</td><td></td></tr>
<tr><td>15
16</td><td>GND</td><td>0</td><td>—</td><td>Connect to ground with minimum inductance. Track length should be kept as short as possible.</td><td></td></tr>
<tr><td>17</td><td>Power Save</td><td>V_{PS}</td><td>—</td><td>Power save control pin can control the ON/SLEEP state with a bias as follows:
<table><tr><th>V_{PS} (V)</th><th>STATE</th></tr><tr><td>2.0 ~ 3.6</td><td>ON</td></tr><tr><td>0 ~ 0.8</td><td>SLEEP</td></tr></table></td><td> 
</td></tr>
<tr><td>18</td><td>GND</td><td>0</td><td>—</td><td>Connect to ground with minimum inductance. Track length should be kept as short as possible.</td><td rowspan="3"></td></tr>
<tr><td>19</td><td>V_{CC}</td><td>2.7 ~
3.6</td><td>—</td><td>Supply voltage pin for the modulator. An internal regulator helps keep the device stable against temperature or V_{CC} variations.</td></tr>
<tr><td>20</td><td>GND</td><td>0</td><td>—</td><td>Connect to ground with minimum inductance. Track length should be kept as short as possible.</td></tr>
</table>

*1: $V_{CC/2}$ DC bias must be supplied to I, $\overline{I}$, Q, $\overline{Q}$.

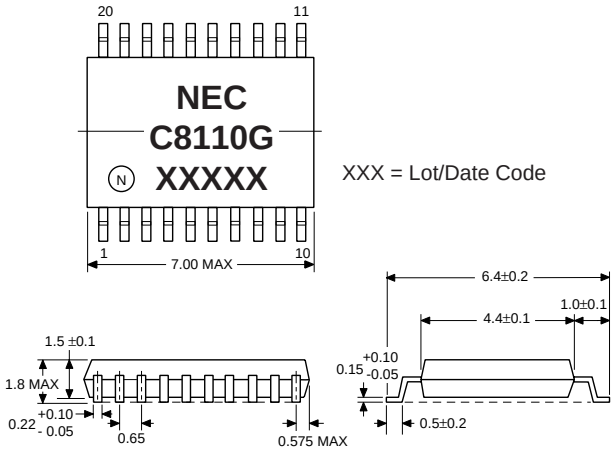
EXPLANATION OF INTERNAL FUNCTIONS

Block	Function/Operation	Block Diagram
90° PHASE SHIFTER	Input signal from the LO input is sent to a T-type flip-flop through a frequency doubler. The output signal from the T-type F/F is changed to the same frequency as the LO input with a quadrature phase shift of 0°, 90°, 180°, or 270°. These circuits provide self phase correction for proper quadrature signals.	
BUFFER AMPLIFIER	Buffer amplifiers for each phase signal are sent to each mixer.	
MIXER	The signals from the buffer amps are quadrature modulated with two double-balanced mixers. High accurate phase and amplitude inputs are realized to provide excellent image rejection.	
ADDER	Output signals from each mixer are added and sent through a final amplifier.	



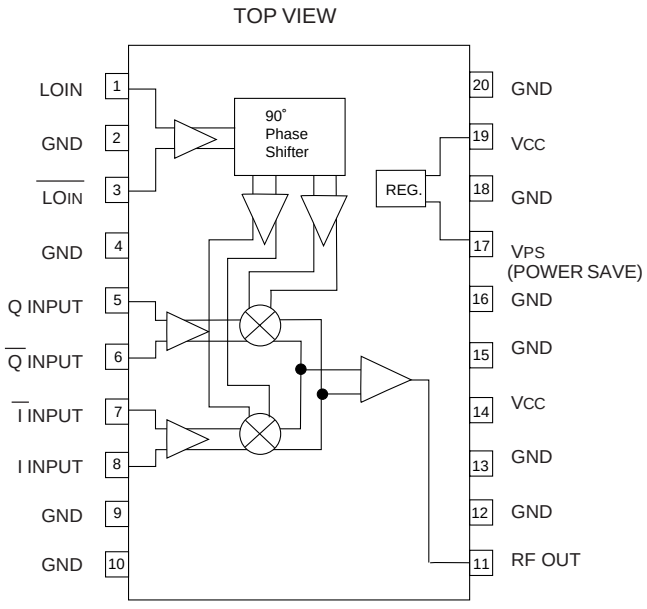
OUTLINE DIMENSIONS (Units in mm)

PACKAGE OUTLINE S20 (SSOP20)



Note:
All dimensions are typical unless otherwise specified.

INTERNAL BLOCK DIAGRAM



ORDERING INFORMATION

PART NUMBER	QTY
UPC8110GR-E1	2.5 K/Reel